Serial No.: 09/663,021
Group Art Unit: 2815

REMARKS

Claim Rejections - 35 USC §112

The Examiner states:

> "The specification on for example page 4 with references to figures 1 and 2 describe channels 101 and 102 as openings. The second channel is described as having an opening 106 with side walls 109. The channel 102 is taught to be filled with conductive material."

The references to FIGs. 1 and 2 (PRIOR ART) show the channels 101 and 102 to be structures as indicated by the leader lines to the outside of the structures, as would be known to those having ordinary skill in the art. The channels have barrier layers and seed layers containing a conductive material, as also well known to those having ordinary skill in the art. The second channel 102 is deposited in the opening 106 in the dielectric layer 108 as indicated by the leader line and the sidewalls are 109 as indicated by the leader lines to the inside of the opening 106, as also well known to those having ordinary skill in the art.

The above is known to be well known to those having ordinary skill in the art because it is part of the "damascene" technique described in the Background Art of the Specification, which concludes on page 2, lines 5-6:

> "...damascenes the first conductive material in the first channel openings to form the first channels." [underlining for clarity]

The Examiner continues:

> "With regard to the instant invention shown in figures 3-4 a similar channel or opening is shown as 201 containing a conductive filler material. The conductive filler material in figure 3 looks to be the reduced or etched back as described in line 28 of page 5. The disclosure on page 5 appears to recite that the channel is etched back but if the channel is an opening then the conductive material in the channel is etched back. The specification therefore is confusing regarding an accurate description of the component features of the invention."

Applicants respectfully disagree. As indicated for Specification FIG 3:

> "[s]trictly for ease of understanding, the completed semiconductor wafer 200 can be understood to be the equivalent of the semiconductor wafer 100 taken along th line 3--3."

Thus, it would be obvious to those having ordinary skill in the art that the channel 201 in FIG. 3 relates to a structure and not an opening just as in FIGs. 1 and 2 the channels are structures and not openings. Therefore, it would be obvious to those having ordinary skill in the art that the channel 201 is a structure, which is etched back as shown in FIG. 3.

From FIG. 3, it would be obvious those having ordinary skill in the art that FIG. 4 shows the etched back region being filled by a material 206, which will be further discussed below.

Based on the above, it is respectfully submitted that the manner and process of making and using the invention is disclosed, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains to make and use the invention.

The Examiner continues:

> "The specification on for example page 7 further describes a semiconductor interconnect barrier but teaches use of no semiconductor materials of which said barrier is formed. Therefore It (sic) would not appear to be " semiconductor". What makes it "semiconductor"? The disclosure describes it as a metal barrier that may be formed of copper so describing it as semiconductor appears misdescriptive. It would appear to be a metal interconnect barrier."

Applicants respectfully disagree because those having ordinary skill in the art would recognize that the term "semiconductor interconnect barrier layer" is not misdescriptive because it is a short hand term for a barrier layer for a conductive interconnection in interlayer dielectric layers where the conductive interconnection is used to interconnect semiconductor devices. However, to avoid even potential confusion, these adjectives have been deleted from claims 19 and 20.

Those having ordinary skill in the art would also recognize that a barrier layer would not necessarily be a "metal barrier" since various non-metal compound materials are also used. The broadest claims have been amended by deleting the adjective "metallic" from before barrier material to reflect this fact and to better claim what the Applicants are entitled to claim.

The Examiner continues:

> "Claims 19 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention."

Applicants respectfully request elaboration on this rejection since the above is the entire rejection and the Examiner does not point to any specific failure to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner continues:

> "Claim 10 describes a recessed channel which is confusing because a channel is an opening. The recessed features appears (sic) to be the filling in the channel.
>
> A " semiconductor interconnect" appears to have no material basis in the disclosure.
>
> In claim 19, it is unclear what is meant by a recessed channel in the channel opening. The "channel" in the disclosure on for example pages 4 and 5 are described as openings or trenches."

It is respectfully submitted that as explained above, claims 10 and 19 would not be confusing to those having ordinary skill in the art because it would be obvious to those so skilled that a "channel" is a structure including a barrier layer and a conductive layer, and that a "channel opening" is an opening.

Further, it would be obvious to those having ordinary skill in the art that the Applicants as their own lexicographers have defined a recessed channel to be formed from a conductive material recessed into a barrier layer in a channel opening as explained in Specification page 7, lines 20-23:

> "The conductive material in the first channel 201 is then subject to an etch back by a wet or dry etching. Generally, the predetermined etch back will remove at least as much of the first channel 201 as required for the thickness of a conventional barrier layer to form the recessed first channel 201."

The "semiconductor interconnect" has been addressed above as a descriptor of a barrier layer.

The first paragraph of 35 USC §112 states:

> "The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention." [underlining for clarity]

It is respectfully submitted that, based on the first paragraph of 35 USC §112, the rejections should be withdrawn since those having ordinary skill in the art would understand

the prior art and the Specification would enable any person of ordinary skill in the art to make and use the invention.

Claim Rejections - 35 USC §102

The sequence of the rejections has been modified from that used by the Examiner in the Office Action to conform to the conventional USPTO practice of providing 35 USC §102 rejections first followed by providing 35 USC §103 rejections second.

Claims 1-4 are rejected under 35 USC §102(a) as being anticipated by Zhao et al (USPN 6,100,184, hereinafter "Zhao").

With regard to claims 1-4, it is respectfully submitted that the Applicants' claimed combination, as exemplified in claim 1, has been amended in line with the Examiner's suggestions and now includes the limitation not disclosed in Zhao of:

> "a second barrier layer disposed in said first barrier layer and over said conductive layer..." (underlining added)

The support for the above amendment is best shown in FIG. 5 and explained in Specification page 7, lines 20-23, where the first barrier layer is not removed while the conductive material is removed:

> "The conductive material in the first channel 201 is then subject to an etch back by a wet or dry etching. Generally, the predetermined etch back will remove at least as much of the first channel 201 as required for the thickness of a conventional [second] barrier layer to form the recessed first channel 201." [underlining and insertion for clarity]

Zhao FIG. 16 discloses conductive channels 10 and 29 filling respective dielectric layers 11 and 18 and having respective barrier layers 33 and 34 outside of their respective barrier layers 12 and 28, and also outside of their respective channel openings.

The advantages of the claimed structure over Zhao can be illustrated by a simple example. If the channels were cylindrical, such as a via, the claimed structure would have a sealing area that is a cylinder while Zhao would a sealing area which is a circular ring. Generally, a cylindrical area has a larger sealing area than a circular ring.

It is respectfully submitted Zhao cannot anticipate that claim 1 because the Zhao second barrier layer is not in the Zhao first barrier layer. The Court of Appeals for the Federal Circuit has stated:

> "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" [*emphasis added*] Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co. (730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)(citing Connell v. Sears, Roebuck & Co., 722 F.2d 1542, 220 USPQ 193 (Fed Dir. 1983)))

The dependent claim 2 depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof including a first barrier layer of a metallic barrier material selected from a group of specified materials.

The dependent claim 3 depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof including a second barrier layer of a metallic barrier material selected from a group of specified materials.

The dependent claim 4 depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth in the independent claim from which it depends and claims unobvious combinations thereof including a conductive material selected from a group of specified materials.

Claims 7-10, 13-16, are rejected under 35 U.S.C. 102(a) as being anticipated by Zhao et al:

With regard to claims 7-10 and 13-16, the Examiner states:

> "Zhao et al shows a first barrier layer 28 disposed in a dielectric layer lining, a conductive layer 29 disposed in said barrier layer and a second barrier layer 34 disposed over said layers and totally enclosing said conductive layer. The material recited in the claims are further taught by Zhao et al (see col. 8, line 33, col. 4, lines 63-64, col. 10, line 29, col. 8, lines 23). The steps of providing, forming, removing and depositing are deemed to be inherently taught by Zhao et al." [underlining for clarity]

The Board of Patent Appeals and Interferences stated in *Ex parte* Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990):

> "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte* Levy, supra (emphasis in original) (The Board reversed the examiner's rejection because the examiner did not provide objective evidence or cogent technical reasoning to support the conclusion of inherency.).

It is respectfully submitted that there is no objective evidence or cogent technical reasoning to support the conclusion of inherency in Zhao. To the contrary, it is not possible for the amended limitations now claimed below to read on Zhao:

> "recessing said conductive layer inside said first barrier layer to form a recessed channel; and
> forming a second barrier layer in said first barrier layer over said conductive layer..." [underlining for clarity]

As shown in Zhao FIG. 16, the conductive layers 10 and 29 are coplanar with respective first barrier layers 12 and 28. Further, Zhao specifically teaches away from the second limitation of forming the second barrier layer in the first barrier layer. Zhao's specification teaches using techniques "to selectively deposit" the second barrier layer "atop the exposed metal region" (column 10, lines 19-21) which would include the first barrier layers 12 and 28.

The disadvantage of a deposition process atop the exposed metal region is that it requires accurate location and alignment also over the liner layers (Zhao liner layers 12 and 28). Misalignment will result in the failure of the second barrier layer.

In marked contrast, the Applicants' patent application is titled a "Self-Aligned Semiconductor Interconnect Barrier Layer..." and discloses a self-aligned deposition process which deposits the second barrier layer in the first barrier layer rather than atop it. To be self-aligned, the conductive layer is recessed in the first barrier layer, and the second barrier layer is formed inside the first barrier layer as claimed.

The dependent claims 8 and 14 respectively depend from independent claims 7 and 13, and ar believed to be allowable since they contain all th limitations set forth in the

independent claim from which they depend and claim unobvious combinations thereof including a first barrier layer of a metallic barrier material selected from a group of specified materials.

The dependent claims 9 and 15 respectively depend from independent claims 7 and 13, and are believed to be allowable since they contain all the limitations set forth in the independent claim from which they depend and claim unobvious combinations thereof including a second barrier layer of a metallic barrier material selected from a group of specified materials.

The dependent claims 10 and 16 respectively depend from independent claims 7 and 13, and are believed to be allowable since they contain all the limitations set forth in the independent claim from which they depend and claim unobvious combinations thereof including a conductive material selected from a group of specified materials.

Claims 19 and 20 are rejected under 35 USC §102(a) as being anticipated by Zhao et al (USPN 6,100,184, hereinafter "Zhao").

The Examiner states:

> "Zhao et al shows a first barrier layer 28 disposed in a channel opening of a dielectric layer, a conductive material 29 disposed in said barrier layer in said opening and an interconnect barrier layer 34 disposed over said layers and totally enclosing said conductive material. Said interconnect layer 15 is shown below the surface of the device and therefore recessed below the surface in the channel." [underlining for clarity]

The amendment to claim 20 now moots the above statement for the reasons stated for claim 1. In addition, it is submitted that those having ordinary skill in the art would recognize that "an interconnect barrier" of a barrier material cannot read on an "interconnect layer 15" of a dielectric material; i.e., the former is a conductor and the latter is an insulator.

The Examiner continues:

> "The claims contain method of making characteristics (i.e. self aligned) given no patentable weight in determining the patentability of the final device structure."(sic)

With regard to claims 19 and 20, it is respectfully submitted that these claims are not product by process claims. It is well known to those having ordinary skill in th art that

certain structures in the semiconductor arts have specific structural characteristics. The term "self-aligned" specifies how a structure is located with regard to other structures; e.g., the barrier layer is aligned or in a position by itself over the conductive material. A well known example of this is the "self-aligned silicide" for semiconductor junction to contact connections, which is referred to as a "salicide" indicating that it is located between a semiconductor gate and a shallow trench isolation.

Claims 1-4 are rejected under 35 USC §102(a) as being anticipated by Besser et al (USPN 6,172,421, hereinafter "Besser"). The Examiner states:

> "Besser et al shows a first barrier layer 11 disposed in a channel opening of a dielectric layer, a conductive layer 12 disposed in said barrier layer in said opening and a second barrier layer 15 disposed over said layers and totally enclosing said conductive layer. The material recited in the claims are further taught by Besser et al et al." [underlining for clarity]

With regard to claims 1-4, it is respectfully submitted that the Applicants' claimed combination, as exemplified in claim 1, has been amended to include the limitations not disclosed in Besser of:

> "a conductive material recessed in said first barrier layer in said channel opening to form a recessed channel; and
> a second barrier layer disposed over said conductive layer in said first barrier layer, said second barrier layer of a barrier material..." [underlining for clarity]

The support for the above amendment is in FIG. 5 and in Specification page 7, lines 20-23, supra.

Besser discloses a dielectric layer 10 with an opening having a first barrier layer 11 and a conductive layer 12 in and coplanar with the dielectric layer 10. A metal, titanium 14, which reduces and forms an intermetallic material with the conductive layer 12, is deposited. A rapid thermal anneal is performed to cause the conductive layer 12 and the metal 14 to interact to form a second barrier layer 15 of intermetallic material and the metal 14 is removed. Besser does not recess the conductive layer 12 to form a recessed channel.

As well known to those having ordinary skill in the art, the disadvantage of the above is that rapid thermal anneals must be used sparingly and within a specified thermal budget in the manufacture of semiconductor devices because the rapid thermal ann als affect the

source/drain implantations which are at the heart of the semiconductor devices. As a result, the rapid thermal anneal of Besser must be controlled carefully to provide the second barrier layer 15 to an adequate thickness while not substantially disturbing the thermal budget of the source/drain implantations. Thus, the thickness of the second barrier layer obtainable is limited.

In Applicant's claimed invention, any thickness of the second barrier layer can be obtained, without having to be concerned with the thermal budget, merely by controlling the thickness of the recessed channel.

The dependent claims 2-4 depend from amended independent claim 1 and are believed to be allowable since they contain all the limitations set forth in the independent claim from which they depend and claim unobvious combinations thereof as previously explained.

Claims 19-20 are rejected under 35 USC §102(a) as being anticipated by Besser et al (USPN 6,172,421, hereinafter "Besser").

With regard to claims 19-20, these claims contain the combination of limitations previous discussed with regard to amended claim 1 and are submitted to be allowable for the same reason.

Claims 1-4 are rejected under 35 USC §102(a) as being anticipated by Joshi et al (USPN 5,889,328, hereinafter "Joshi").

> "Joshi et al shows in figure 8, a first barrier layer 28 disposed in a channel opening of a dielectric layer, a conductive layer 16 disposed in said barrier layer in said opening and a second barrier layer 17 disposed over said layers and totally enclosing said conductive layer. The material recited in the claims are further taught by Joshi et al."

Joshi FIG. 8 shows a first barrier layer in an insulator and a second barrier layer over the first barrier layer.

With regard to claims 1-4, it is respectfully submitted that amended claim 1, and dependent claims 2-4, ar not anticipated by Joshi for the same reasons applicable to Zhao, which reasons are incorporated here by reference thereto.

Claims 19 and 20 are rejected under 35 USC §102(a) as being anticipated by Joshi et al (USPN 5,889,328, hereinafter "Joshi").

With regard to claims 19-20, these claims contain the combination of limitations previous discussed with regard to amended claim 1 and are submitted to be allowable for the same reason.

Claims 1, 7, and 13 have been amended to delete an unneeded reference to "said opening" in which the second barrier layer is disposed or formed and the "whereas" clause, which is not required as a limitation.

It is respectfully submitted that claims 1-4, 7-10, 13-16, and 19-20 are not anticipated by Zhao, Besser, and/or Joshi taken singularly under 35 USC §102 or obvious in combination under 35 USC §103.

Claim Rejections - 35 USC §103

Claims 5, 6, 11, 12, 17, and 18 are rejected under 35 USC §103(a) as being unpatentable over Zhao et al (USPN 6,100,184, hereinafter "Zhao") in view of Dubin et al. (USPN 5,695,810, hereinafter "Dubin").

The dependent claims 5, 11, and 17 respectively depend from independent claims 1, 7, and 13, and are believed to be allowable since they contain all the limitations set forth in the independent claim from which they depend and claim unobvious combinations thereof including the first and second barrier layers are of the same metallic barrier material.

More specifically, Applicants respectfully submit that absent a teaching suggesting that the material of the first and second barrier layers be the same, such a conclusion is <u>not</u> obvious. Absent some teaching, this conclusion then is an application of an "obvious to try" standard, which is an inappropriate standard of obviousness as indicated in *In re* Lindell, 385 F.2d 435, 155 USPQ 521 (C.C.P.A. 1967), which criticized this test.

> "These are, perhaps, the obvious areas to try. But resulting inventions are not necessarily obvious. Serendipity is not a prerequisite to patentability. Our view is that "obvious to try" is not a sufficiently discriminatory test."

The dependent claims 6, 12, and 18 respectively depend from independent claims 1, 7, and 13, and are believed to be allowable since they contain all the limitations set forth in the independent claim from which they depend and claim unobvious combinations thereof including the first and second barrier layers having substantially the same thickness.

In particular, the Applicants respectfully submit that it would not have been obvious to modify Zhao in view of Dubin. The Examiner stated in the Office Action page 3, next to last paragraph, that:

> "Zhao et al fails to express a particular thickness of the second barrier layer but refers to a particular application for deposition technique which is related to the Dubin et al patent which teaches forming said layers in the range of thickness as those discussed by Zhao et al with regard to the first barrier layer. Therefore it would have been obvious to one having ordinary skill in the art to...form the second barrier layer of the same thickness as the first. The ordinary artisan would have been motivated to modify Zhao et al because Zhao et al suggests use of the techniques taught by Dubin et al which would include similar layer thickness of the second layer to that of the first." [deletions for clarity]

Applicants respectfully disagree. Zhao Col. 10, lines 26-30, refers to Dubin, and discloses that the first barrier layer in Zhao is of approximate thickness of 100-1000 angstroms (Col. 8, lines 30-35), but Dubin does not teach forming a second barrier layer in the range of thickness as those discussed by Zhao for the first barrier layer. Dubin only discloses the composition and method of depositing a barrier layer and does not disclose the thickness to which a barrier layer should be formed. Therefore, both Zhao and Dubin fail to disclose the thickness of the second barrier layer.

Further, the first barrier layer in Zhao is "conformally deposited" (Col. 8, lines 19-21 and 36-38), while the second barrier layer in Zhao is selectively deposited (Col. 10, lines 18-20). Because the two barrier layers are deposited with different methods, in different places, and with different inherent problems, the Applicants respectfully submit that it would not be obvious to modify Zhao in view of Dubin to render the Applicants' invention obvious.

Serial No.: 09/663,021
Group Art Unit: 2815

Based on the above, claims 5, 6, 11, 12, 17, and 18 are respectfully submitted as being allowable under 35 USC §103(a) as being unobvious and patentable over Zhao in view of Dubin.

The other references cited by the Examiner showing the prior art have been considered and are not believed to disclose, teach, or suggest, either singularly or in combination, Applicants' invention as claimed.

Tuttle (USPN 6,417,561) cited by the Examiner as "having second recessed barriers located in a channel region" was filed February 28, 2001, after Applicant's Application, which was filed September 15, 2000.

Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1-20 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 01-0365 and please credit any excess fees to such deposit account.

Respectfully submitted,

Mikio Ishimaru
Registration No. 27,449

The Law Offices of Mikio Ishimaru
1110 Sunnyvale-Saratoga Rd., Suite A1
Sunnyvale, CA 94087
Telephone: (408) 738-0592
Fax: (408) 738-0881
Date: June 13, 2003